Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1 (Currently Amended). A method for prioritizing access to a shared resource in a digital system having a plurality of devices vying for access to the shared resource, comprising the steps of:

organizing an address space of the shared resource into address space regions;

assigning individual access priority values to a plurality of the address space regions;

initiating an access request by a first device of the plurality of devices, wherein the access request specifies a target address within the address space of the shared resource;

providing an access priority value with the access request, such that the access priority value corresponds to an access priority value assigned to an address space region selected by the target address; and

arbitrating between multiple pending requests to the shared resource for access to the shared resource based at least in part by using the access priority value assigned to each pending request.

2 (Original). The method of Claim 1, wherein the shared resource is a memory circuit and wherein the step of assigning comprises assigning an access priority value to an address space region according to a program or data stored within the address space region.

3 (Original). The method according to Claim 2, wherein a program task occupies several address space regions, and wherein the step of assigning assigns a first access priority value to a first one of the several address space regions and assigns a different access priority value to a second one of the several address space regions.

PAGE 4/11 * RCVD AT 3/14/2005 7:13:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/3 * DNIS:8729306 * CSID:9726649606 * DURATION (mm-ss):04-32

4 (Original). The method according to Claim 2, wherein a plurality of program tasks occupy a single address space region, and wherein the step of assigning assigns a single access priority value to the single address space region.

5 (Original). The method according to Claim 1, wherein the step of assigning comprises the steps of:

starting a program task;

determining an access priority value specified by the program task;

allocating an address space region for the program task; and

assigning the access priority value specified by the program task to the address space region allocated for the program task.

6 (Original). The method according to Claim 1, wherein the step of providing comprises the steps of:

storing at least a portion of the individual access priority values in page entries associated with a memory management unit (MMU); and

accessing a selected page entry in the MMU in response to the target address specified by the access request to obtain an access priority value.

7 (Original). The method according to Claim 1, wherein an access priority value assigned to an address space region is related to an execution priority value of a program task to which the address space region is allocated.

8 (Currently Amended). A digital system comprising:

a shared resource;

a plurality of devices connected to access the shared resource;

a plurality of memory management units (MMU) each connected to receive an address from a respective one of the plurality of devices, wherein each MMU has storage circuitry for storing a plurality of page entries and each page entry has an access priority field, each MMU being operable to output an access priority value associated with ~~in~~-

PAGE 5/11 * RCVD AT 3/14/2005 7:13:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/3 * DNIS:8729306 * CSID:9726649606 * DURATION (mm-ss):04-32

~~response to~~ a received address; and

arbitration circuitry connected to receive a request signal from each of the plurality of devices and an associated access priority value from each MMU, wherein the arbitration circuitry is operable to schedule access to the shared resource according to the access priority values.

9 (Original). The digital system according to Claim 8, wherein one or more of the plurality of MMUs comprise a translation lookaside buffer (TLB).

10 (Original). The digital system according to Claim 8, wherein the shared resource is a memory circuit.

11 (Original). The digital system according to Claim 8, wherein the shared resource is a bus, and further comprising a plurality of memory mapped resources connected to the bus.

12 (Original). The digital system according to Claim 8 being a wireless communication device, wherein at least one of the plurality of devices is a processor (CPU), further comprising:

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.

PAGE 6/11 * RCVD AT 3/14/2005 7:13:31 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/3 * DNIS:8729306 * CSID:9726649606 * DURATION (mm-ss):04-32